

LDMOS transistor, and the solid lines denote the Vd-Id characteristics of the LDMOS transistor according to some embodiments of the present invention. The results were obtained at gate voltages of 2V, 3V, 4V, and 5V.

[0056] As shown in FIG. 10, the breakdown voltages BV of the conventional LDMOS transistor and the LDMOS transistor according to some embodiments of the present invention are both 200V. However, in the conventional LDMOS transistor, the on-breakdown voltage (on-BV) is less than about 180V when the gate voltage is higher than about 2V, and the on-breakdown voltage is decreased to about 135V when the gate voltage reaches about 5V. According to some embodiments of the present invention, the on-breakdown voltage is not decreased until the gate voltage reaches about 4V but is decreased to about 170V when the gate voltage is about 5V, which is considerably higher than the on-breakdown voltage (135V) of the conventional technique. Furthermore, a saturation current of the LDMOS transistor according to some embodiments of the present invention when the gate voltage is about 5V is greater than that of the conventional LDMOS transistor.

[0057] Thus, according to some embodiments of the present invention, a current flow path at the surface of a drift region in a LDMOS transistor may be distributed due to a high impurity density retrograde region formed within the drift region. As such, a current path between the source and drain regions may be displaced from the surface of the drift region adjacent the gate electrode. Accordingly, current characteristics and/or breakdown voltage characteristics of the LDMOS transistor may be enhanced, and SOA characteristics of the LDMOS transistor can be improved without increasing a length of the drift region.

[0058] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims.

That which is claimed:

1. A metal-oxide semiconductor (MOS) transistor, comprising:

a semiconductor substrate including a source region and a drain region adjacent a surface of the substrate and a drift region between the source region and the drain region, the drift region having an impurity concentration distribution such that a peak impurity concentration of the drift region is displaced from the surface of the substrate.

2. The transistor of claim 1, wherein the drift region comprises a retrograde region below the surface of the substrate and separated therefrom by a predetermined distance, wherein the peak impurity concentration of the drift region is provided in a portion of the retrograde region.

3. The transistor of claim 2, wherein an impurity concentration of the drift region decreases between a portion of the drift region adjacent the surface of the substrate and the retrograde region.

4. The transistor of claim 2, wherein an impurity concentration of the drift region decreases between the retrograde region and a surface of the substrate opposite the source and drain regions.

5. The transistor of claim 2, wherein the portion of the retrograde region having the peak impurity concentration is displaced from the surface of the substrate by a distance of about 1 micrometer (μm) to about 3 micrometer (μm).

6. The transistor of claim 2, wherein the retrograde region laterally extends at the predetermined distance below the surface of the substrate and under the drain region.

7. The transistor of claim 6, and wherein an edge of the retrograde region is aligned with an edge of the drain region.

8. The transistor of claim 2, wherein the semiconductor substrate further comprises a body region adjacent the surface of the substrate between the drift region and the source region, wherein the retrograde region is separated from the body region.

9. The transistor of claim 8, wherein the source region, the drain region, and the drift region comprise a first conductivity type, and wherein the body region comprises a second conductivity type.

10. The transistor of claim 2, further comprising:

a field insulating layer on the surface of the substrate adjacent the drift region and between the source region and the drain region,

wherein the retrograde region laterally extends at the predetermined distance below the surface of the substrate and under the drain region and the field insulating layer.

11. The transistor of claim 1, further comprising:

a gate insulating layer on the surface of the substrate adjacent the drift region and between the source region and the drain region; and

a gate electrode on the gate insulating layer.

12. The transistor of claim 1, wherein the substrate is a semiconductor-on-insulator (SOI) substrate including a buried insulating layer adjacent a surface of the substrate opposite the source region and the drain region.

13. A metal-oxide semiconductor (MOS) transistor, comprising:

a semiconductor substrate;

a source region of a first conductivity type adjacent a surface of the substrate;

a drain region of the first conductivity type adjacent the surface of the substrate;

a drift region of the first conductivity type in the substrate between the source region and the drain region, the drift region including a retrograde region therein below the surface of the substrate, the retrograde region having an impurity concentration greater than an impurity concentration of a portion of the drift region adjacent the surface of the substrate;

a body region of a second conductivity type in the substrate adjacent the surface thereof between the drift region and the source region and configured to provide a channel region between the source region and the drift region; and

a gate electrode on the channel region.

14. A metal-oxide semiconductor (MOS) transistor, comprising:

a semiconductor substrate including a source region and a drain region adjacent a surface of the substrate and a